CLAIMS

What is claimed is:

1. A computer program product comprising program instructions stored by a computer-readable medium for directing operations of a computer during specification of an integrated circuit, comprising:

first computer program code that enables a user to specify the existence of uncertainty in a least one circuit; and

second computer program code that automatically implements the specified uncertainty as at least one programmable circuit.

2. A computer program product as in claim 1, further comprising third computer program code that optimizes an implementation of the at least one programmable circuit in view of at least one predetermined performance constraint.

3. A computer program product as in claim 1, where said first computer program code implements an Uncertain Function that is used in place of a logic function or operator.

4. A computer program product as in claim 3, where said Uncertain Function comprises an at least

partly unspecified Boolean logic function with multiple inputs and multiple outputs.

5. A computer program product as in claim 3, where said Uncertain Function comprises a selectable Boolean logic function having an input used to select one of a plurality of fully specified logic functions.

6. A computer program product as in claim 3, where said Uncertain Function comprises a Boolean logic function having a set of input parameters used to determine a specific logic function to be implemented.

7. A computer program product as in claim 3, where said first computer program code implements an Uncertain Function Assertion for imposing at least one constraint on the Uncertain Function.

8. A computer program product as in claim 7, where said Uncertain Function Assertion comprises at least one of an Input Assertion that uses a Boolean expression to specify a constraint on an input value and an Output Assertion that uses a Boolean expression to specify a constraint on an output value.

9. A computer program product as in claim 7, where said Uncertain Function Assertion comprises an Input/Output Assertion that uses a Boolean expression to specify a constraint on a relation between input and output values.

10. A computer program product as in claim 7, where said Uncertain Function Assertion comprises a Dependency Assertion for defining which inputs determine which outputs.

11. A computer program product as in claim 3, where said first computer program code implements an Uncertain Constant having a predetermined number of bits.

12. A computer program product as in claim 1, where said first computer program code implements an Uncertain Register as a register having a programmable size within a specified range.

13. A computer program product as in claim 1, where said integrated circuit is implemented at least in part as a hardwired application specific integrated circuit (ASIC), and where said at least one programmable circuit is implemented as a field programmable gate array (FPGA).

14. A computer program product as in claim 1, where said integrated circuit is implemented at least in part as a hardwired application specific integrated circuit (ASIC), and where said at least one programmable circuit is implemented as an ASIC in combination with a programmable memory component that provides at least one control input to said programmable circuit.

15. A computer program product as in claim 2, where said third computer program code operates to simplify a circuit network obtained by operation of said second computer program code by using logic synthesis optimizations in accordance with at least one assertion.

16. A computer program product as in claim 1, where said at least one assertion comprises at least one of Input, Output and Input/Output assertions that introduce constraints that reduce the complexity of a final circuit implementation, and Dependency assertions that eliminate inputs from selected outputs.

17. A computer program product as in claim 2,where said third computer program code operates to map a circuit network obtained by operation of said first and second program code to at least one specific logic technology.

18. A computer program product as in claim 17, where said integrated circuit is implemented at least in part as a hardwired application specific integrated circuit (ASIC), and where said at least one programmable circuit is implemented as a field programmable gate array (FPGA), and where said third computer program code operates to map FPGA components to an FPGA section of the integrated circuit and to map ASIC components to an ASIC section of the integrated circuit.

19. A computer program product as in claim 2, where said third computer program code selects a specific technology for implementing the at least one programmable circuit in view of the at least one performance constraint.

20. A computer program product as in claim 2, where said at least one performance constraint comprises circuit timing imposed by clock signal constraints.

21. A computer program product as in claim 2, where optimizing comprises a consideration of required circuit area versus operational performance.

22. A computer program product as in claim 1, further comprising additional computer program code for implementing a hardware bring-up operation wherein a hardware correspondence, derived from an Uncertain Synthesis process that is implemented using said first computer program code and said second computer program code, is read to establish a mapping of specific values to a hardware implementation of the integrated circuit, where specific values are read for each uncertain hardware entity and are used to implement the entity in the hardware.

23. A computer program product as in claim 22, where the Uncertain Synthesis process uses at least one of an Uncertain Function, an Uncertain Register, an Uncertain Constant and an Uncertain Assertion, and where the hardware comprises one of: an application specific integrated circuit (ASIC) in combination with a field programmable gate array (FPGA), an ASIC in combination with a programmable memory, a FPGA, an ASIC in combination with a programmable memory and a FPGA, and an ASIC that uses flip-flops for programmability.

24. A computer program product as in claim 2, where said third computer program code operates to optimize programmable logic using dependency assertions and analyzes specified input dependencies of logic components, disconnects non-dependant inputs, and applies minimization methods to reduce a resulting logic implementation.

25. A system for specification of an integrated circuit, comprising:

at least one data processor coupled to a user interface; and

a memory storing computer program code for directing operation of said at least one data processor for enabling a user to specify, using said user interface, the existence of uncertainty in a least one circuit, and for automatically implementing the specified uncertainty as at least one programmable circuit.

26. A system as in claim 25, said memory further storing computer program code for optimizing an implementation of the at least one programmable circuit in view of at least one predetermined performance constraint.

27. A system as in claim 25, where said computer program code implements an Uncertain Function that is used in place of a logic function or operator, where said Uncertain Function comprises at least one of an at least partly unspecified Boolean logic function with multiple inputs and multiple outputs, a selectable Boolean logic function having an input used to select one of a plurality of fully specified logic functions, and a Boolean logic function having a set of input parameters used to determine a specific logic function to be implemented.

28. A system as in claim 27, where said computer program code further implements an Uncertain Function Assertion for imposing at least one constraint on the Uncertain Function, said Uncertain

Function Assertion comprising an Input Assertion that uses a Boolean expression to specify a constraint on an input value, an Output Assertion that uses a Boolean expression to specify a constraint on an output value, an Input/Output Assertion that uses a Boolean expression to specify a constraint on a relation between input and output values and a Dependency Assertion for defining which inputs determine which outputs.

29. A system as in claim 27, where said computer program code further implements an Uncertain Register as a register having a programmable size within a specified range.

30. A system as in claim 27, where said computer program code further implements an Uncertain Constant having a predetermined number of bits.

31. A system as in claim 25, further comprising additional computer program code executed by the same or a different data processor for implementing a hardware bring-up operation wherein a hardware correspondence, derived from an Uncertain Synthesis process that is implemented using said computer program code, is read to establish a mapping of specific values to a hardware implementation of the integrated circuit, where specific values are read for each uncertain hardware entity and are used to implement the entity in the hardware.

32. A system as in claim 31, where the Uncertain Synthesis process uses at least one of an Uncertain Function, an Uncertain Register, an Uncertain Constant and an Uncertain Assertion.

33. A system as in claim 31, where the hardware comprises one of: an application specific integrated circuit (ASIC) in combination with a field programmable gate array (FPGA), an ASIC in combination with a programmable memory, a FPGA, an ASIC in combination with a programmable memory and a FPGA, and an ASIC that uses flip-flops for programmability.

34. A method to specify an integrated circuit, said integrated circuit comprising a hardwired specific logic technology portion and a programmable specific logic technology portion, comprising:

generating a hybrid logic network by mapping each uncertain logic function to an abstract programmable logic element implementation thereof and by mapping each known logic function to a technology-independent logic element implementation thereof;

simplifying the hybrid logic network using logic synthesis optimizations;

mapping the simplified hybrid logic network to a specific technology by mapping the abstract programmable logic element implementation to the specific programmable logic technology and the technology-independent logic element implementation to the specific logic technology; and

optimizing the mapped network in accordance with at least one performance constraint.

35. A method as in claim 34, where generating comprises using integrated circuit specification language extensions that comprise an Uncertain Function used in place of a logic function or

operator, where said Uncertain Function comprises at least one of an at least partly unspecified Boolean logic function with multiple inputs and multiple outputs, a selectable Boolean logic function having an input used to select one of a plurality of fully specified logic functions, and a Boolean logic function having a set of input parameters used to determine a specific logic function to be implemented.

36. A method as in claim 35, where said integrated circuit specification language extensions further comprise an Uncertain Function Assertion for imposing at least one constraint on the Uncertain Function, said Uncertain Function Assertion comprising an Input Assertion that uses a Boolean expression to specify a constraint on an input value, an Output Assertion that uses a Boolean expression to specify a constraint on an output value, an Input/Output Assertion that uses a Boolean expression to specify a constraint on a relation between input and output values and a Dependency Assertion for defining which inputs determine which outputs.

37. A method as in claim 35, where said integrated circuit specification language extensions further comprise an Uncertain Register as a register having a programmable size within a specified range.

38. A method as in claim 35, where said integrated circuit specification language extensions further comprise an Uncertain Constant having a predetermined number of bits.

39. A method as in claim 35, where said hardwired specific logic technology portion comprises an application specific integrated circuit (ASIC) portion, and where said programmable specific logic

technology portion comprises a field programmable gate array (FPGA) portion.

40 A computer program product comprising program instructions stored by a computer-readable medium for directing operations of a computer to implement an integrated circuit, comprising:

first computer program code enabling a user to specify the existence of uncertainty in a least one circuit that comprises the integrated circuit;

second computer program code that automatically maps the specified uncertainty into at least one circuit; and

third computer program code that optimizes an implementation of the at least one circuit in view of at least one predetermined performance constraint.

41. A computer program product as in claim 40, where said first computer program code implements an Uncertain Function that is used in place of a logic function or operator, where said Uncertain Function comprises at least one of an at least partly unspecified Boolean logic function with multiple inputs and multiple outputs, a selectable Boolean logic function having an input used to select one of a plurality of fully specified logic functions, and a Boolean logic function having a set of input parameters used to determine a specific logic function to be implemented.

42. A computer program product as in claim 41, where said first computer program code implements

an Uncertain Function Assertion for imposing at least one constraint on the Uncertain Function, where said Uncertain Function Assertion comprises at least one of an Input Assertion that uses a Boolean expression to specify a constraint on an input value, an Output Assertion that uses a Boolean expression to specify a constraint on an output value, an Input/Output Assertion that uses a Boolean expression to specify a constraint on a relation between input and output values, and a Dependency Assertion for defining which inputs determine which outputs.

43. A computer program product as in claim 40, where said first computer program code implements an Uncertain Register as a register having a programmable size within a specified range.

44. A computer program product as in claim 40, where said first computer program code implements an Uncertain Constant having a predetermined number of bits.

45. A computer program product as in claim 40, where said integrated circuit is implemented at least in part as a hardwired application specific integrated circuit (ASIC), and where said at least one programmable circuit is implemented as at least one of a field programmable gate array (FPGA) and an ASIC in combination with a programmable random access memory that provides at least one control input to at least one of said programmable circuit.

46. A computer program product as in claim 40, where said third computer program code operates to simplify a circuit network obtained by operation of said second computer program code by using logic synthesis optimizations in accordance with at least one assertion that comprises at least one of

Input, Output and Input/Output assertions that introduce constraints that reduce the complexity of a final circuit implementation, and Dependency assertions that eliminate inputs from selected outputs, and selects a specific technology for implementing the at least one programmable circuit in view of the at least one performance constraint.

47. A computer program product as in claim 40, where said at least one performance constraint comprises at least one of circuit timing imposed by clock signal constraints, and a consideration of required circuit area versus operational performance.

48. A computer program product as in claim 40, where said third computer program code operates to optimize programmable logic using dependency assertions and analyzes specified input dependencies of logic components, disconnects non-dependant inputs, and applies minimization methods to reduce a resulting logic implementation.

49. A computer program product as in claim 40, further comprising computer program code for implementing a hardware bring-up operation wherein a hardware correspondence, derived from an Uncertain Synthesis process that is implemented using at least said first computer program code and said second computer program code, is read to establish a mapping of specific values to a hardware implementation of the integrated circuit, where specific values are read for each uncertain hardware entity and are used to implement the entity in the hardware.

50. A computer program product as in claim 49, where the Uncertain Synthesis process uses at least

one of an Uncertain Function, an Uncertain Register, an Uncertain Constant and an Uncertain Assertion.

51. A computer program product as in claim 49, where the hardware comprises one of: an application specific integrated circuit (ASIC) in combination with a field programmable gate array (FPGA), an ASIC in combination with a static random access memory (SRAM) for programmability, a FPGA, an ASIC in combination with an SRAM and a FPGA, and an ASIC that uses flip-flops for programmability.